**PRACTICE PROBLEMS BASED ON ADDRESSING MODES-**

1. The most appropriate matching for the following pairs is-

**Column-1:**

X: Indirect addressing

Y: Immediate addressing

Z: Auto decrement addressing

**Column-2:**

1. Loops

2. Pointers

3. Constants

1. X-3, Y-2, Z-1
2. X-1, Y-3, Z-2
3. X-2, Y-3, Z-1
4. X-3, Y-1, Z-2

Ans: (c)

1. In the absolute/direct addressing mode:
2. The operand is inside the instruction
3. The address of the operand is inside the instruction
4. The register containing the address of the operand is specified inside the instruction
5. The location of the operand is implicit

Ans: (b)

1. Which of the following addressing modes are suitable for program relocation at run time?
2. Absolute addressing
3. Base addressing
4. Relative addressing
5. Indirect addressing

1. 1 and 4
2. 1 and 2
3. 2 and 3
4. 1, 2 and 4

Ans: (c)

1. What is the most appropriate match for the items in the first column with the items in the second column?

**Column-1:**

X: Indirect addressing

Y: Indexed addressing

Z: Base register addressing

**Column-2:**

1. Array implementation

2. Writing relocatable code

3. Passing array as parameter

1. X-3, Y-1, Z-2
2. X-2, Y-3, Z-1
3. X-3, Y-2, Z-1
4. X-1, Y-3, Z-2

Ans: (a)

1. Which of the following addressing modes permits relocation without any change whatsoever in the code?
2. Indirect addressing
3. Indexed addressing
4. Base register addressing
5. PC relative addressing

Ans: (d)

1. Consider a three-word machine instruction-

ADD A[R0], @B

The first operand (destination) “A[R0]” uses indexed addressing mode with R0 as the index register. The second operand (source) “@B” uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is-

1. 3
2. 4
3. 5
4. 6

Ans: (B)  
  
**Explanation**: In Indexed addressing mode, the base address is already in the instruction i.e., A and to fetch the index data from R0 no memory access is required because it’s a register So to fetch the operand only 1 memory cycle is required. Indirect Addressing mode requires 2 memory cycles only

1. Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?
2. Immediate Addressing
3. Register Addressing
4. Register Indirect Scaled Addressing
5. Base Indexed Addressing

Ans: (D)

1. The memory locations 1000, 1001 and 1020 have data values 18, 1 and 16 respectively before the following program is executed.

|  |  |  |
| --- | --- | --- |
| MOVI | Rs, 1 | Move immediate |
| LOAD | Rd, 1000(Rs) | Load from memory |
| ADDI | Rd, 1000 | Add immediate |
| STOREI | 0(Rd), 20 | Store immediate |

Which of the statements below is TRUE after the program is executed?

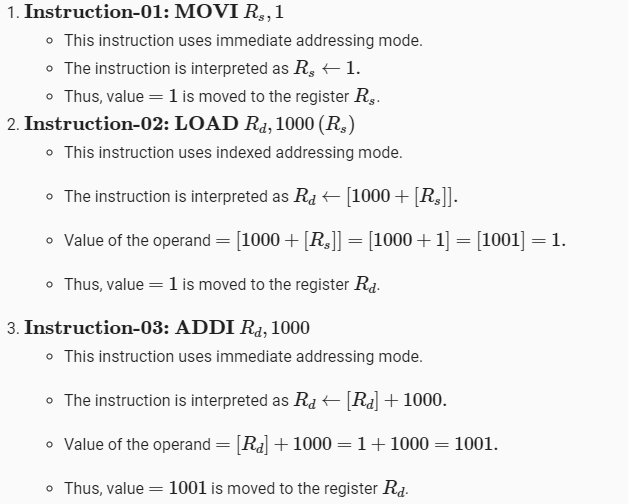
1. Memory location 1000 has value 20
2. Memory location 1020 has value 20
3. Memory location 1021 has value 20
4. Memory location 1001 has value 20

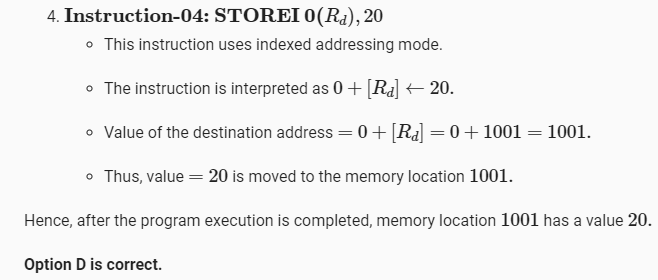
Ans: (d)

Explanation: Before the execution of the program, the memory contents are-

Table

Description automatically generated





1. Consider the following memory values and a one-address machine with an accumulator, what values do the following instructions load into accumulator?

* Word 20 contains 40
* Word 30 contains 50
* Word 40 contains 60
* Word 50 contains 70

Instructions are-

1. Load immediate 20
2. Load direct 20
3. Load indirect 20
4. Load immediate 30
5. Load direct 30
6. Load indirect 30

 Ans: (a) 20 (b) 40 (c) 60 (d) 30 (e) 50 (f) 70

1. Consider a hypothetical processor with an instruction of type LW R1, 20 (R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for the operand in memory?

a) Immediate AM

* 1. Register Indirect Scaled AM
  2. Base Indexed AM
  3. Register AM

Ans: **(D)**  
  
Base Index Addressing, as the content of register R2 will serve as the index, and 20 will be the Base address.

11. The addressing mode/s, which uses the PC instead of a general-purpose register is\_\_\_\_\_\_

a) Indexed with offset

b) Relative

c) Direct

d) Both Indexed with offset and direct

Ans: (b)

* + - 1. The addressing mode which makes use of in-direction pointers is \_\_\_\_\_\_  
         a) Indirect addressing mode  
         b) Index addressing mode  
         c) Relative addressing mode  
         d) Offset addressing mode

Ans: (a)  
Explanation: In this addressing mode, the value of the register serves as another memory location and hence we use pointers to get the data.

* + - 1. The instruction, Add #45, R1 does \_\_\_\_\_\_\_  
         a) Adds the value of 45 to the address of R1 and stores 45 in that address  
         b) Adds 45 to the value of R1 and stores it in R1  
         c) Finds the memory location 45 and adds that content to that of R1  
         d) None of the mentioned

Ans: b  
Explanation: The instruction is using immediate addressing mode hence the value is stored in the location 45 is added.

14. Add #45, when this instruction is executed, the following happen/s \_\_\_\_\_\_\_  
a) The processor raises an error and requests for one more operand  
b) The value stored in memory location 45 is retrieved and one more operand is requested  
c) The value 45 gets added to the value on the stack and is pushed onto the stack  
d) None of the mentioned

Ans: (b)

15. In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is \_\_\_\_\_\_  
a) EA = 5+R1  
b) EA = R1  
c) EA = [R1]  
d) EA = 5+[R1]

Ans: (d)

16. When we use auto increment or auto decrements, which of the following is/are true?  
1. In both, the address is used to retrieve the operand and then the address gets altered  
2. In auto increment, the operand is retrieved first and then the address altered  
3. Both of them can be used on general purpose registers as well as memory locations  
a) 1, 2, 3  
b) 2  
c) 1, 3  
d) 2, 3

Ans: (d)

Explanation: In the case of, auto increment the increment is done afterward and in auto decrement the decrement is done first.

17. The addressing mode, where you directly specify the operand value is \_\_\_\_\_\_\_  
a) Immediate  
b) Direct  
c) Definite  
d) Relative

Ans: (a)

18. The effective address of the following instruction is MUL 5(R1, R2).  
a) 5+R1+R2  
b) 5+(R1\*R2)  
c) 5+[R1]+[R2]  
d) 5\*([R1]+[R2])

Ans: (c)

Explanation: The addressing mode used is base with offset and index.

19.  \_\_\_\_\_ addressing mode is most suitable to change the normal sequence of execution of instructions.  
a) Relative  
b) Indirect  
c) Index with Offset  
d) Immediate

Ans: a

Explanation: The relative addressing mode is used for this since it directly updates the PC.

20. An instruction SUB 3030

a) Subtracts 3030 to the value in Accumulator and stores the result in the memory location 3030

b) Subtracts the value in memory location 3030 to the value in Accumulator and stores the result in Accumulator

c) Subtracts 3030 to the value in Accumulator and stores the result in Accumulator

d) None of the above

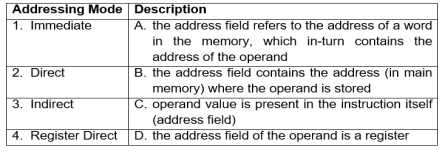
Ans: (b)

21. How many bits of opcode is required to implement a CPU with 10 arithmetic and logical instructions, 2 control instructions, and 5 data transfer instructions?

1. 2
2. 3
3. 4
4. 5

Ans: (d)

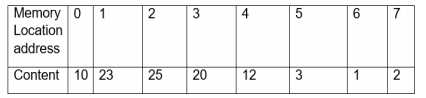
22. Which of the following options represents the correct matching?



1. 1->A; 2->D; 3->C; 4->B;
2. 1->C; 2->B; 3->D; 4->A;
3. 1->C; 2->B; 3->A; 4->D;
4. 1->A; 2->D; 3->B; 4->C;

Ans: (c)

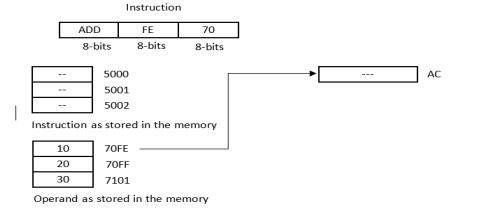
23. Consider an example of memory organization as shown in the figure below. Which value will be loaded into the accumulator when the instruction “LOAD DIRECT 3” is executed?



1. 3
2. 25
3. 12
4. 20

Ans: (d)

24. Consider a CPU with 8-bit data bus and 16-bit address bus. The memory is byte organized. Consider the instruction format with one operand. Length of the instruction is three bytes and the first byte indicates the op-code. Second byte indicates the lower eight bits address and third byte indicates the higher eight bits address. Consider the instruction “ADD FE 70”. This instruction adds the content of memory location to accumulator. The instruction is stored in consecutive memory location starting from memory location 5000H. We assume that Accumulator initially has the value of 20. In the figure given below, what are the values in Memory Locations 5000, 5001, 5002 and Accumulator after the instruction ADD FE 70 is executed.



a) 5000=ADD, 5001=FE, 5002=70, and Accumulator=30

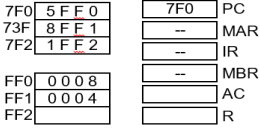
b) 5000=ADD, 5001=70, 5002=FE, and Accumulator=30

c) 5000=ADD, 5001=70, 5002=FE, and Accumulator=40

d) 5000=ADD, 5001=FE, 5002=70, and Accumulator=40

Ans: (a)

25. The instruction LDA FF0 (machine code of LDA is 5) is stored in location 7F0. The contents 1 point in memory location FF0 are loaded into accumulator. After its execution, accumulator stores value 8. The figure below shows a snapshot of the registers and their contents. Immediately after the fetch cycle of the 1st instruction (LDA FF0), the values in MAR, IR and MBR are:



a) MAR=FF0, IR=5FF0

b) MBR=5FF0 MAR=7F0, IR=5FF0,

c) MBR=0008 MAR=7F0, IR=5FF0

d) MBR=5FF0 MAR=FF1, IR=5FF0, MBR=7F0

Ans: (c)